A Simplified Method for Interconnect Time and Frequency Compliance Testing Using PCI Express 3.0, Tektronix 8300 TDR with IConnect® and Gigaprobes® TDR Probe

"Measurement Techniques for Transceiver Differential Impedance and SDD11/21 S-Parameters"

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Transceiver differential impedance and SDD11/21 S-parameter measurements can streamline time and frequency compliance when using 8 Gb/s third generation PCI Express (PCIe 3.0). The step-by-step technique described in this application note leverages the nearly controlled impedance path in a Tektronix TDR instrument and the Gigaprobes high-bandwidth TDR probe to reduce calibration overhead compared with a vector-network-analyzer approach.

PCI Express 3.0 (PCIe) has replaced PCI in most chip-to-chip applications, including pathways crossing circuit boards and cable connections. PCIe is a highly scalable architecture that provides from one to 16 dual-simplex lanes in a PCIe link. In multi-lane applications the data stream is divided among available lanes and transmitted nearly simultaneously at the lane rate. The fastest PCIe applications are typically used in graphics, connecting 16 lanes of high-speed, high-resolution graphical data between a system's chipset and a graphics processor.

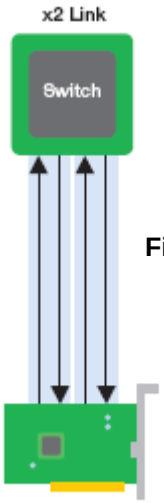


Fig. 1

This application note will use a cookbook approach to describe how to extract time and frequency domain measurements of a lane in a PCIe 3.0 link. We will use a Tektronix DSA8300 mainframe and two 80E08 TDR sampling modules to make the requisite differential TDR (Time Domain Reflectometry) and TDT (Time Domain Transmission) measurements. IConnect® waveform processing will be used to display impedance and SDD21/11 insertion/return loss S-parameters. The GigaProbes® 30 GHz 100 ohm balanced TDR probe is used to probe each differential PCIe transceiver lane. Results will be evaluated in terms of compliance with PCIe 3.0 standards for impedance and bandwidth parameters.

Figure 1 Illustrates the PCIe 3.0 architecture. The 8 Gb/s transfer rates for the third generation PCIe embeds the clock in the data stream, but also couples a reference clock to drive the PLL reference input on the receiver.

These parametric measurements on the interconnect system are necessary since, at 8 Gb/s data rates, analog signal anomalies have a greater impact on signal integrity and quality than ever before. Signal pathways consisting of circuit board traces, vias, connectors, and cabling will exhibit higher levels of noise, losses and reflections with the increasing data rate to 8Gb/s.

Gigabit Speeds

With each increase in transfer rates of the standards, the UI shrinks and the tolerances in transmitter signal quality and receiver sensitivity become tighter. Low-voltage differential signals and multi-level signaling are more vulnerable to signal integrity issues, differential skew, noise and inter-symbol interference (ISI) as speeds increase. There is also greater susceptibility to timing problems, impedance discontinuities between transmitter and receiver, and system level interaction between hardware and software. Multi-lane architectures amplify design complexity and potential for lane skew timing violations and crosstalk.

Jitter

Today's higher data rates and embedded clocks mean greater susceptibility to jitter, degrading bit error rate (BER) performance. Deterministic Jitter can come from many sources in the system such as crosstalk, simultaneous switching effects and power supply noise, channel inter-symbol interference, and other regularly occurring interference signals. With faster rates, multi-lane architectures and more compact designs, there are more opportunities for all these events to affect data transmission in the form of signal jitter.

Transmission Line Effects

The signal transmitter, conductor pathways and receiver constitute a serial data network. Buried in that network are distributed capacitance, inductance and resistance that have diverse effects on signal propagation as frequencies increase. Transmission line effects rise from this distributed network and can significantly impact signal quality and lead to data errors.

Compliance Testing
Compliance testing for serial standards requires the measurement of many parameters such as TX jitter, eye height and width, RX jitter tolerance, rise and fall time, return loss, impedance, skew, and often many other parameters. Measurement of return and insertion loss and reflections on connectors, cables and other pathways will be the area of focus for this application note. Not all measurements are required for compliance with every standard. Test points are specified in the standard's compliance test document or the specification itself.

Time and Frequency Testing of an 8Gb/s PCIe 3.0 Channel
For this measurement example, we chose channel PE3_S2_P2_Rx[P/N]15 on the PCIeGen3 Channel to make the differential TDR/T measurements and the following channel and port assignments (**Fig. 2**) were used. To assure we had the TDR channel connected to the correct TDT channels we drew a simple schematic and labeled each leg of the differential line of the odd mode signal set. We then attach a unique colored cable tie to each of the TDR modules and the connecting cables. This simple procedure will eliminate connection errors.

Fig. 2

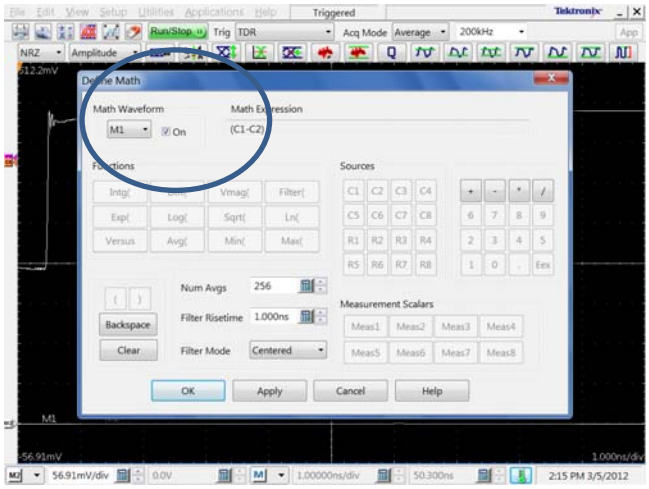
GigaProbes® TDR differential connections to Tektronix 80E10 TDR Plug-in		PCIe Gen3 compliance board SMP connection to Tektronix 80E10 Sampling plug-in
Positive TDR pulse (CH1) **BLUE**	⟷	Positive Pulse (CH3) **Pink**
Negative TDR pulse (CH2) **Yellow**	⟷	Negative Pulse (CH4) **Orange**

To make it easier to process the differential waveform sets, the Tektronix DSA 8300 math function was used to add and subtract the positive and negative odd mode TDR differential waveform set and to create one waveform to be used as the IConnect® reference waveform, differential TDR waveform and TDT waveform from which the SDD11 return loss and SDD21 will be extracted.

After the TDR math function and time base is established, the instrument settings are stored in IConnect®. If it is necessary to repeat the measurement the scope can be setup quickly by recalling the settings. We gave the following name to our instrument setup: **Instrument setup name**: DSA8200_Iconnect_PCIeG3_Scope_Settings.set

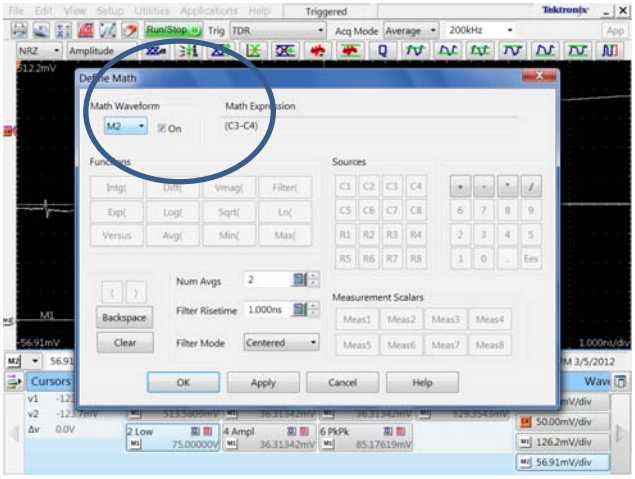
The following math definitions in **Fig. 3** were used on the DSA8300 Scope to create one differential TDR waveform:
Math1=C1-C2

Fig. 3



The following math definitions **Fig 4** were used on the DSA8300 Scope to create one differential Sampling waveforms:
Math2=C3-C4

Fig. 4

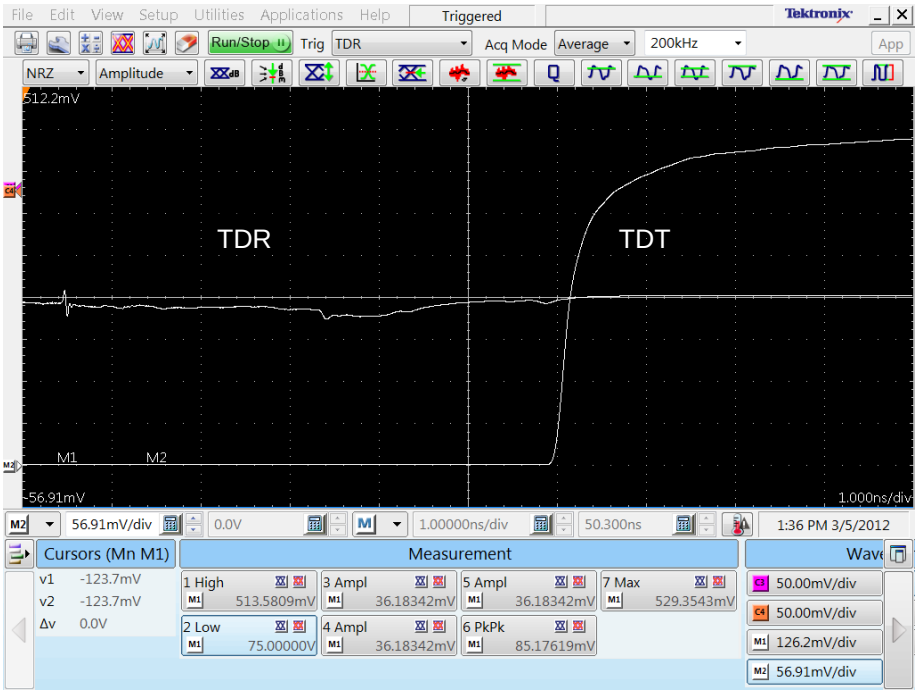


Capturing Differential TDR/T and Reference Waveforms with DSA8300 Oscilloscope

A Tektronix DSA8300 oscilloscope screenshot of the TDR (Math1) and TDT (Math2) waveforms when the GigaProbes® is touching down on the test pads is shown in **Fig. 5** below.

1. Start the “Acquisition” in “Sample Mode” initially to verify that all the probes are touching the pads.
2. After the GigaProbes® pad touches are verified, turn on averaging (~128 samples). This is activated in the “acquisition mode” to increase the dynamic range of the S-parameters and set the “record length” to 2000 points and increase the Delta T time measurement resolution.
3. IConnect® will acquire the TDR and TDT waveforms shown in **Fig. 5** below.

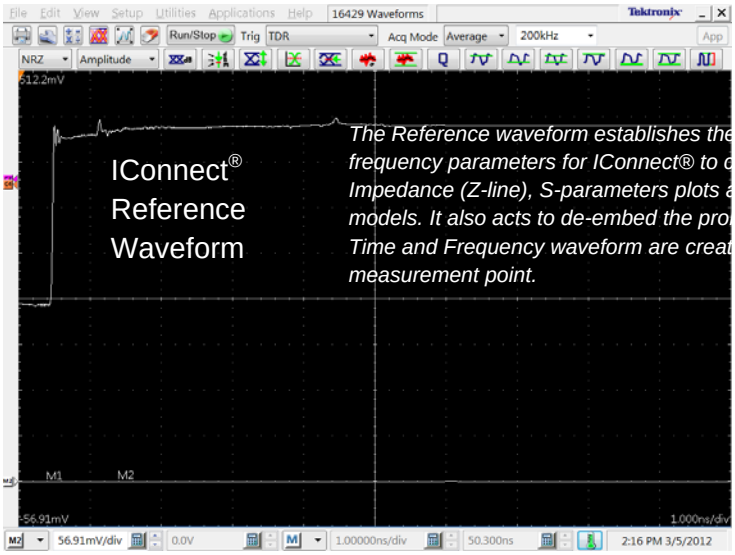
Fig. 5



After the TDR and TDT are acquired by IConnect®:

1. Capture a reference open TDR signal by lifting the GigaProbes® off the pads (**Fig. 6**).
2. Then acquire the waveform in the IConnect® "waveform viewer." We capture the Reference waveform last because the time base has been established to adequately view the TDR and TDT waveforms.

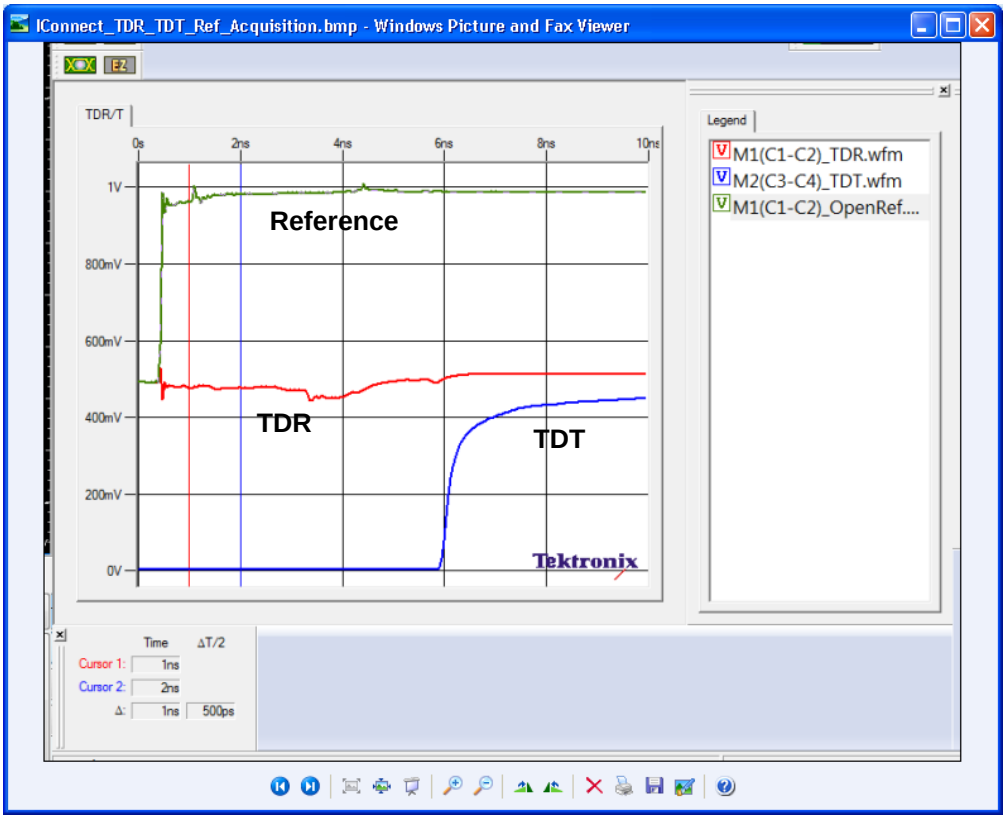
Fig. 6



Capturing Differential TDR/T and Reference Waveforms with IConnect

The screen shot in **Fig. 7** below shows all three waveform signals (TDR, TDT, reference) acquired in IConnect® "waveform view." The TDR waveform is **red**, TDT waveform is **blue** and the reference open waveform is **green**.

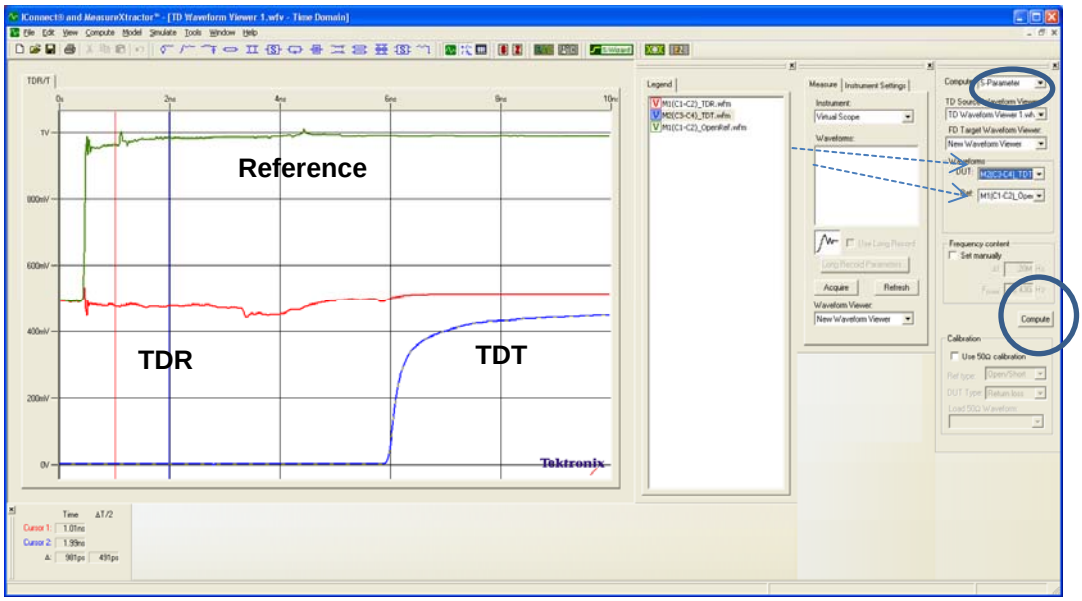
Fig. 7



After the waveforms are captured in the IConnect® “TD Waveform viewer”:

1. Display the Compute Window menu (view/ computation window).
2. Refer to the “waveforms” menu (**Fig. 8**) and select the DUT (M2 (C3-C4) _TDT) and Ref (M1(C1-C2)_OpenRef) waveforms captured from the DSA803 mainframe.
3. In the “Compute” window, select S-parameters.
4. The S-parameter function will be used to extract the differential insertion loss Sdd21 by pressing the “Compute” button.
5. IConnect® will create and display the Sdd21 insertion loss S-parameter plot in a new “FD waveform viewer”.

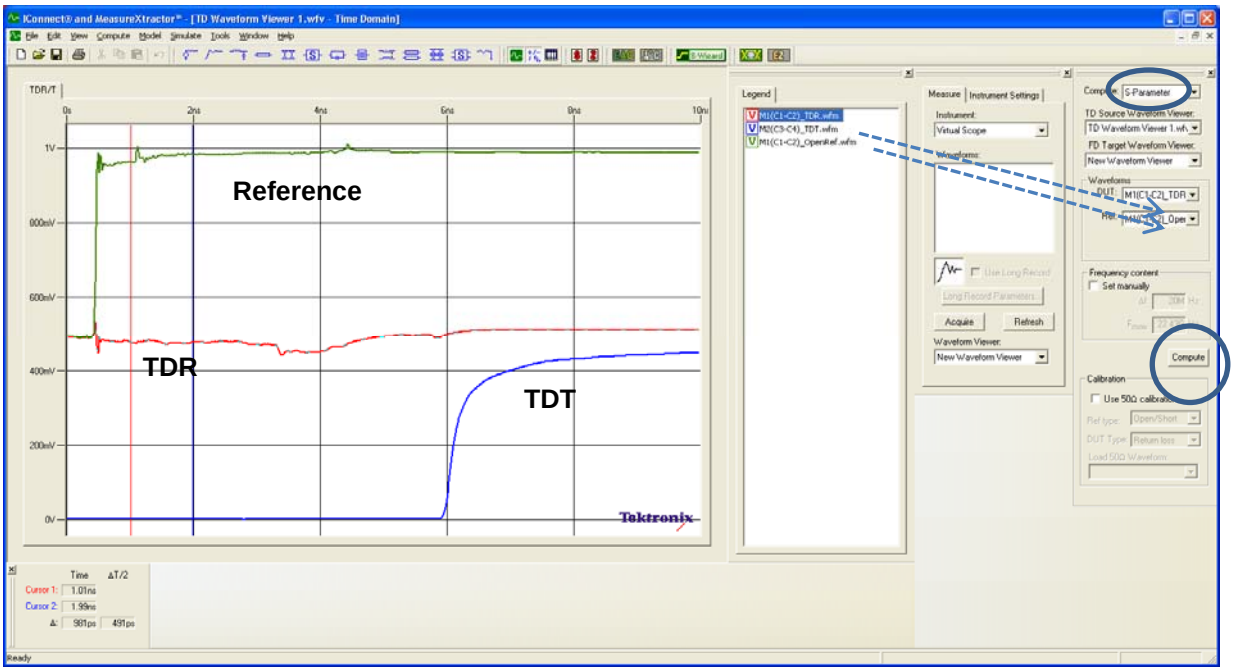
Fig. 8



To create the SDD11 return loss S-parameters:

1. Select the TDR waveform M1 (C1-C2)_TDR in the Waveforms computation box in (Fig 9) and use the same open reference waveform M1(C1-C2)_OpenRef again.
2. Press the “Compute” button.
3. IConnect® places the SDD11 return loss S-parameter plot in the same FD waveform viewer as the SDD21 insertion loss S-parameter plot.

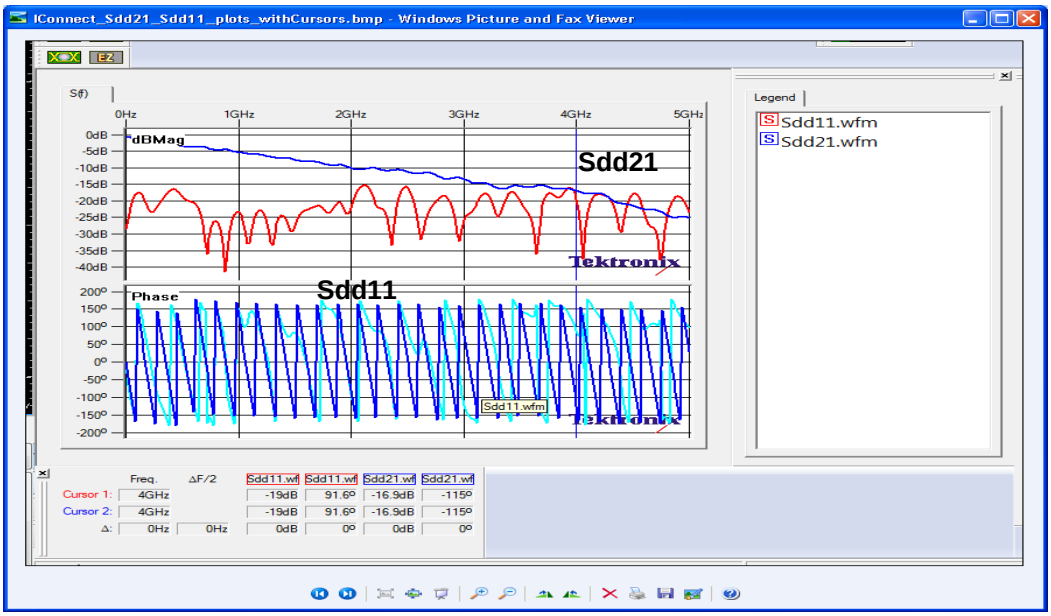
Fig. 9

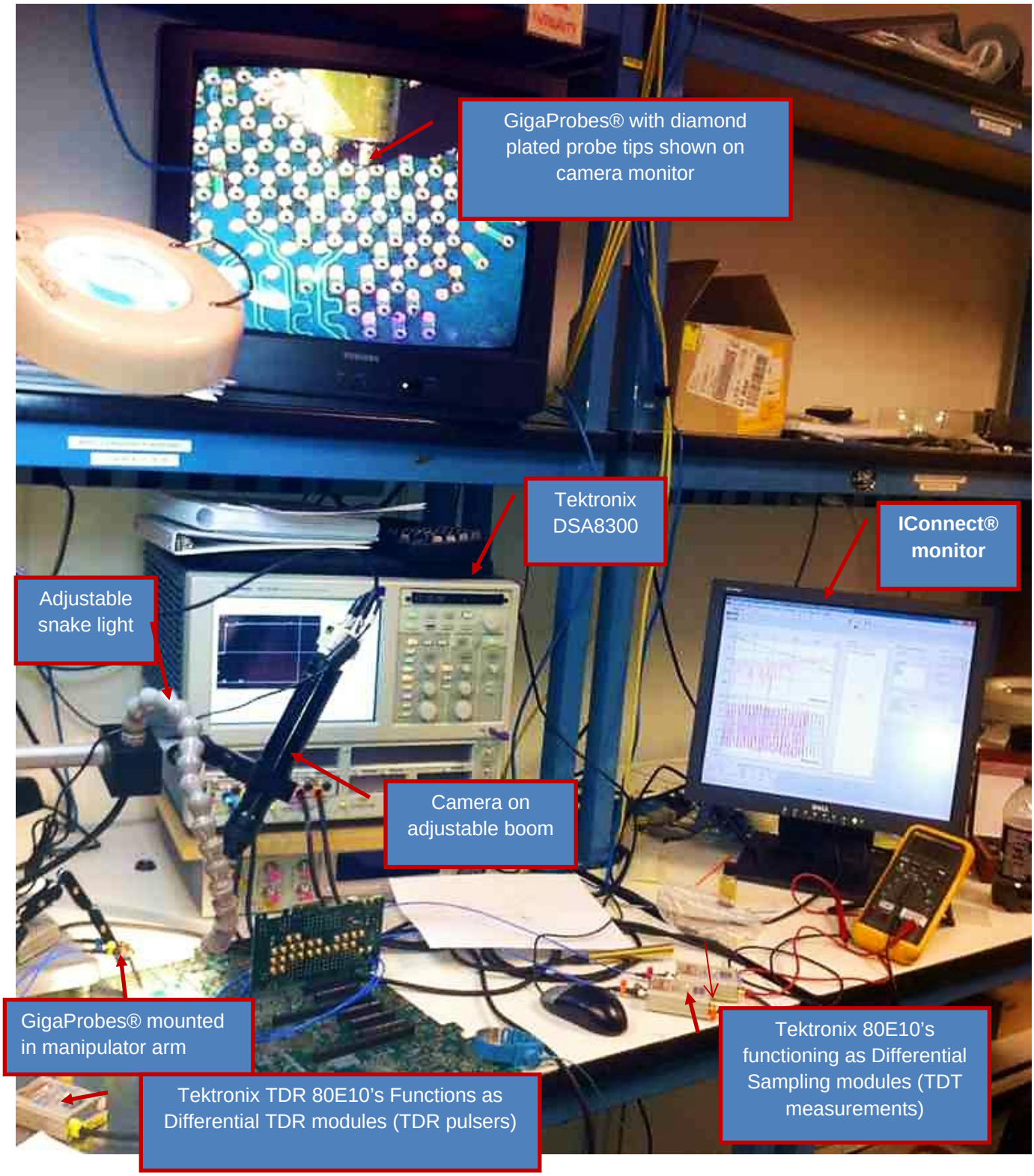


Displaying Sdd21/11 S-parameters

The IConnect® FD waveform viewer screen shot below in **Fig. 10** shows the insertion loss (Sdd21) **blue**, return loss (Sdd11) **red** and phase for both S-parameters. The cursors are set at 4 GHz for PCIe Gen3. Total Insertion loss for this channel @4Ghz =-16.9dB, Return Loss @ 4 GHz = -19dB.

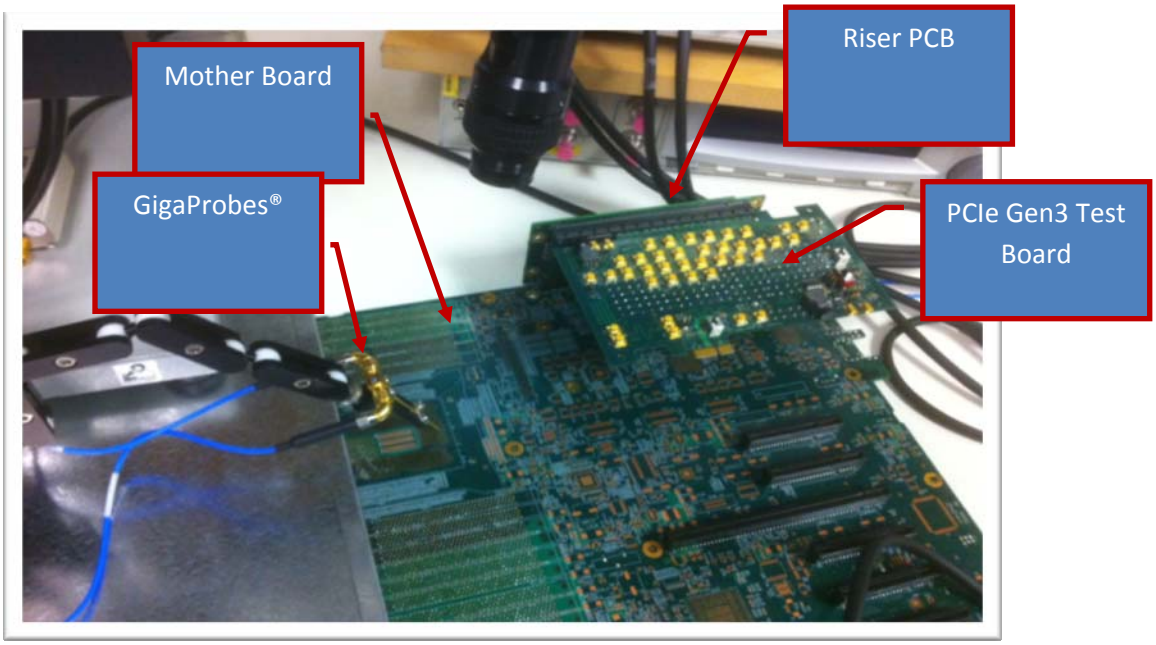
Fig. 10



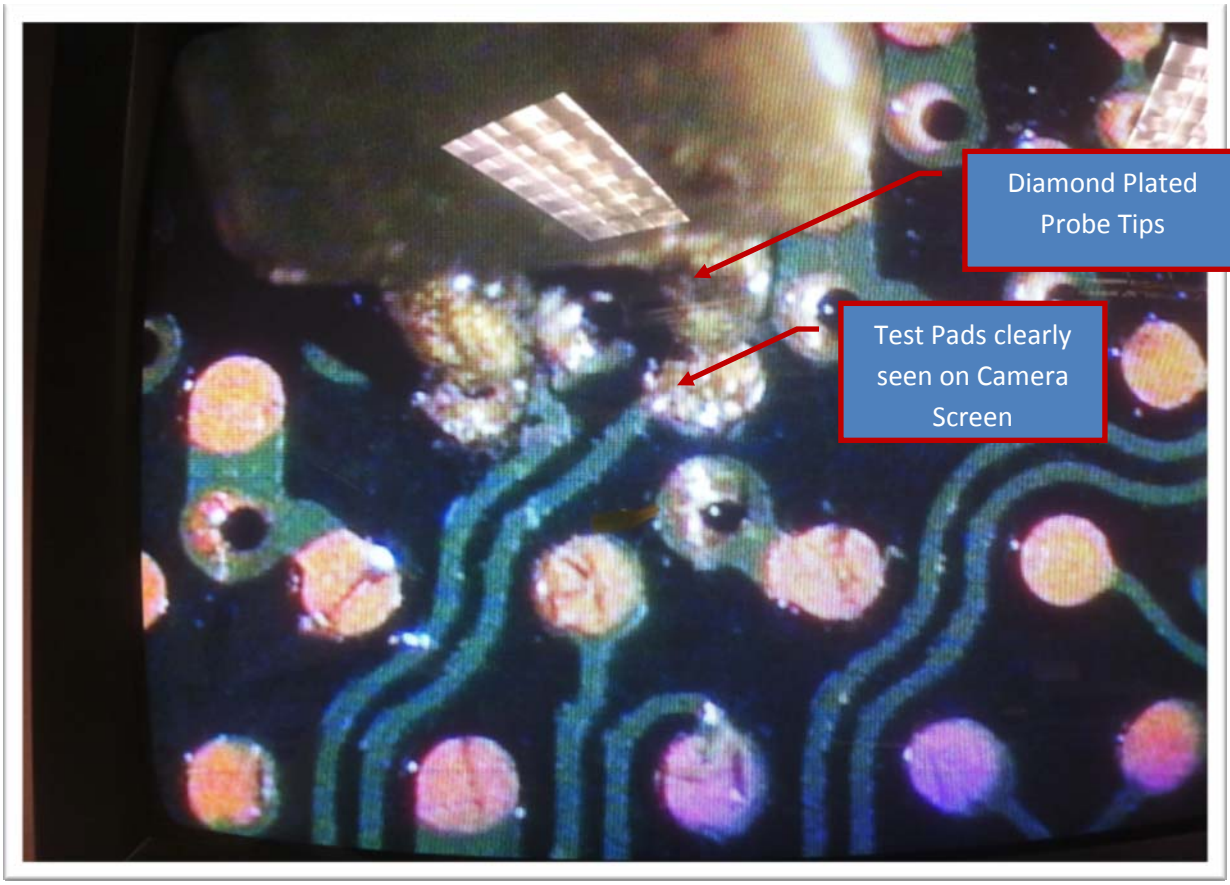


Test equipment and fixtures for making time and frequency measurements on each of the PCIe 3.0 transceiver lines is shown above. Using a camera system to magnify the test pads and guide the probe tips significantly reduces miss-probes and increases productivity. The monitor shows magnified GigaProbes® tips touching down on 40 mil pitch pads.

Expanded view of GigaProbes® probing the PCIe 3.0 test platform:



GigaProbes® touching down on pads test pads is shown below. (*Note: room lights are reflected in camera image.)*



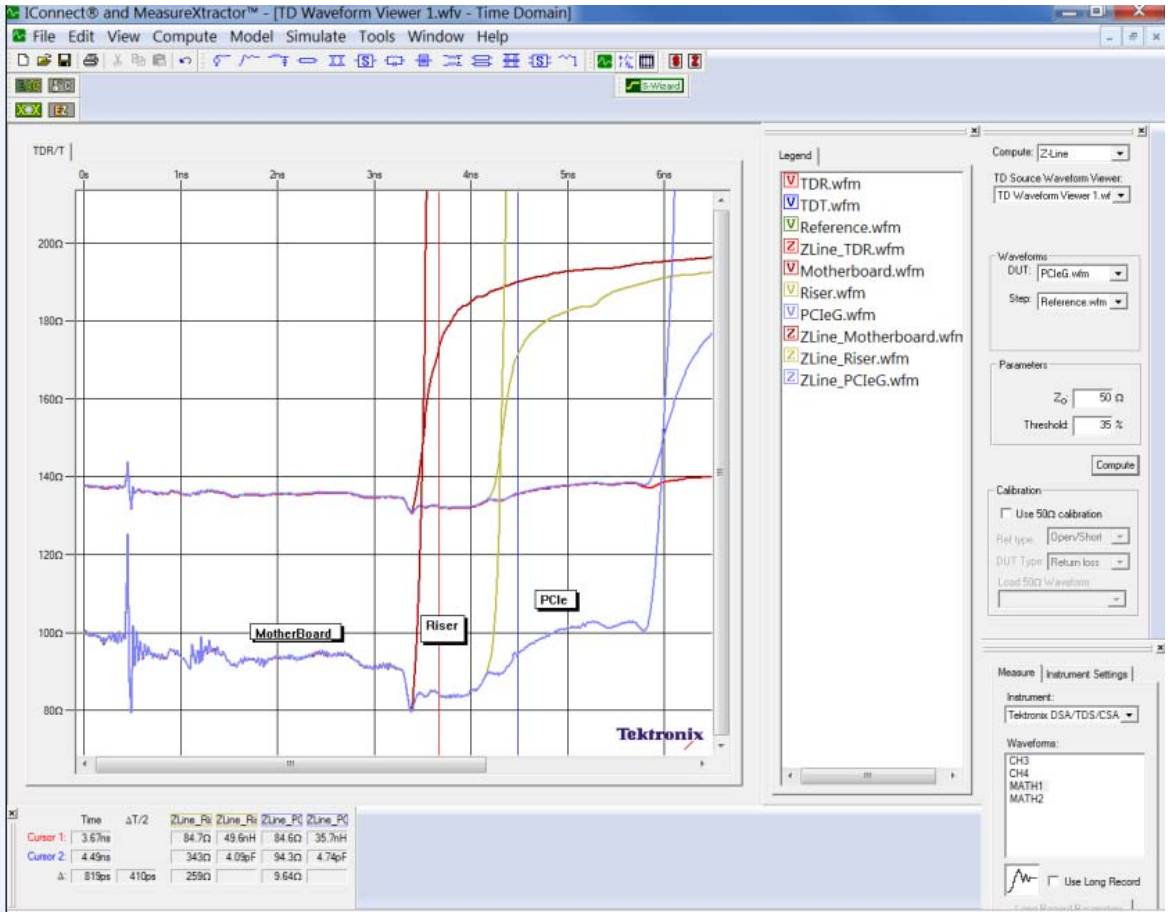
A good example of how IConnect® can be used to determine impedance discontinuities in different sections of the PCIe 3.0 interconnect system illustrated in **Fig 11** below. This differential impedance plot was taken from the test pads on the motherboard, which travel to the PCIe riser card and end at the PCIe 3.0 card.

The trace path segmentation in **Fig. 11** can be achieved as follows:

1. Remove both the riser and PCIe boards, probing the PCB motherboard pads and executing an impedance Z-line profile with IConnect.
2. Then attach the “Riser” board to the PCB motherboard and TDR the pads on the motherboard again to create a Z-line impedance of the PCB and Riser path.
3. Attach the PCIe Gen3 board and repeat the process.

Each trace should concatenate, creating one differential Z-line impedance trace in the TD Waveform Viewer. At this point it is easy to see the entire differential path, how the impedance changes within each board and if the impedance in any segment is out of specification. You can see exactly which board is contributing to the impedance discontinuity. For example, we are starting out at 100 ohms on the motherboard; we see the riser board has an impedance dip of around 85 ohms and the impedance returns to 100 ohm on the PCI3 board. It turn out that 85 ohms is an Intel’s standard impedance specification for this board, and when measured, the board is within specification. If we are measuring too much return loss or getting too much deterministic jitter we can return to the segmented impedance waveforms to look for opportunities to optimize the impedance path were possible.

Fig. 11



Equipment Used

Test Equipment:
Tektronix 8300 Mainframe
80E10 (two for differential TDR and Two as a differential receiver)
www.tektronix.com

SI Software:
IConnect® software
www.tektronix.com

TDR/T Probes:
GigaProbes® TDR probes (DVT30-1MM)
www.gigaprobes.com / www.gigaprobestek.com

Fixturing:

- CCD/ analog camera system on boom mount
- Snake light and light intensity control unit
- Two GP2 manipulators with vacuum mount.
- 2'x2' metal plate for mounting
- Vacuum based manipulators
- Vacuum pump

Summary

The TDR and TDT measurements were converted to SDD11 return loss and SDD21 insertion loss S-parameters. The S-parameters were correlated with VNA measurements to verify their accuracy. Segmented TDR measurements of the interconnect system can be used to increase the physical location resolution if any area of the interconnect path is found to be out of tolerance. Unwarranted impedance discontinuities can lead to excessive determinist jitter and ISI errors.

It is very productive to use a camera and flexible light system with the GigaProbes® mounted in a multi-axis manipulator because it provides a clear image of the probe tips to accurately place them on the test pads. Being able to view the pads of the GigaProbes® reduces design verification time and reduced miss probes. We used a metal plate to cover the large PCB to allow a place to put the vacuum base of the manipulator providing a solid contact, preventing it from moving while probing. By clearly labeling all the cables and sampling plugins with color coded ties minimized connection errors.

Purpose	Standard	Governing Body	Websites
Chip-to-chip PCI Express® (PCIe)	PCI Express® (PCIe)	PCI-SIG www.pcisig.org Rapid I/O Trade Association	www.pcisig.org www.rapidio.org

For Further Information
DVT Solutions, LLC maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers using the GigaProbes® and are using our probes with the latest TDR or VNA for analysis of high speed interconnect technology. Please visit **www.gigaprobes.com or www.gigaprobestek.com**

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References
Tektronix – "The Basics of Serial Data Compliance and Validation Measurements"